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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/036,838	12/31/2001	Chuan-Yu Wu	67,200-412	4947

7590 08/25/2004

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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/036,838	WU ET AL.	
	Examiner	Art Unit	
	Zhuo H Li	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,11-14 and 21* is/are rejected.

7)☒ Claim(s) *5-10 and 15-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office action is in response to the Response field on July 30, 2004, which claims 1-21 is pending and claims 22-29 have been cancelled.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-4, 11-14 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zheng (US PAT. 6,195,303).

Regarding claim 1, Zheng disclosures a method in a memory device (340, figure 3) having a bank of N memory blocks (col. 3 line 41 through col. 4 line 15), the method comprising the steps of generating an address for a first one of the N memory blocks as a current first possible refresh block, for refreshing at least a portion of one of possible refresh blocks (col. 7 line 17 through col. 8 line 14), checking for contention between the current first possible refresh block and an externally generated access to one of the N memory blocks (col. 5 line 51 through col. 6 line 9 and col. 9 lines 21-34), i.e., via the comparator (734, figure 7), permitting the externally generated access to the one of the N memory blocks during a certain interval and refreshing the at least portion of the current first possible refresh block during the curtain interval responsive to the memory block of the externally generated access not contending with the current first possible refresh block, i.e., using the multiplexer (732, figure 7) to select either the external access or the internal refreshing operation as an output based on the result of the comparator, (col. 7 line 17 through col. 8 line 14 and col. 9 lines 21-34 and col. 12 line 34-37). Although Zheng does not clearly disclosures the step of generating address for a current second one of the N memory blocks as a current second possible refresh block, Zheng teaches each of the row control circuit (720, figure 7) in the refresh control circuit (700, figure 7) are able to receive an refresh control signal to provide a refresh address generator and perform a refresh operation in corresponding memory bank (col. 8 line 40 through col. 9 line 34), in addition, Zheng teaches the refresh control circuit can support concurrent memory access and refresh of remaining no-active memory sections, and multiple memory banks can be refreshed at any particular moment concurrently (col. 9 line 66 through col. 10 line 15), thus, Zheng teaches using a row control circuit for each memory bank allows for maintenance of a separate refresh address

for each memory bank (col. 8 line 58 through col. 9 line 6). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize the computer system of Zheng is able to generating address for a current second one of the N memory blocks as a current second possible refresh block.

Regarding claim 2, Zheng disclosures the method further comprising the step of permitting the externally generated access to the one of the N memory blocks during a certain interval, and refreshing the at least portion of the current second possible refresh block during the certain interval responsive to the following: 1) the memory block of the externally generated access contending with the current first possible refresh block and, 2) the current first and second possible refresh blocks being different ones of the N memory blocks (col. 7 line 17 through col. 8 line 14), i.e., refresh control circuits can be allow for memory access and refresh, concurrently, on different sets of rows of the memory, (col. 8 lines 29-39).

Regarding claim 3, Zheng disclosures the method further comprising the step of permitting the externally generated access to the one of the N memory blocks during a certain interval, and initiating an idle external access interval responsive to the following: 1) the memory block of the externally generated access contending with the current first possible refresh block, and 2) the current first and second possible refresh blocks being a same one possible refresh block, and refreshing the one possible refresh block during the idle external access interval, (col. 6 lines 21-41, and col. 11 lines 23-56).

Regarding claim 4, Zheng disclosures the method further comprising the step of deferring the external access until a certain interval responsive to the following: 1), the memory block of the externally generated access contending with the current first possible refresh block, and 2),

the current first and second possible refresh blocks being a same one possible refresh block, i.e., using a comparator (634, figure 6) to compare the external address and the internally generated refresh address, and provides the control signal wherein the control signal is asserted if the external address is the same as the internal address, (col. 7 line 17 through col. 8 line 14), refreshing the one possible refresh block before the certain interval, and permitting the externally generated access to the one of the N memory blocks during the curtain interval, i.e., using the multiplexer (732, figure 7) to select either the external access or the internal refreshing operation as an output based on the result of the comparator (col. 7 line 17 through col. 8 line 14 and col. 9 lines 21-34 and col. 12 line 34-37).

Regarding claim 11, the limitations of the claim are rejected as the same reasons set forth in claim 1.

Regarding claim 12, the limitations of the claim are rejected as the same reasons set forth in claim 2.

Regarding claim 13, the limitations of the claim are rejected as the same reasons set forth in claim 3.

Regarding claim 14, the limitations of the claim are rejected as the same reasons set forth in claim 4.

Regarding claim 21, Zheng disclosures a memory apparatus (100, figure 1) comprising a memory array (200, figure 2) segmented into N memory blocks (col. 3 line 41 through col. 4 line 25), first and second address generators, i.e., generator (730, figure 7) in each row control logic respond to corresponding memory banks respectively, wherein the first address generator is operable to generated an address of a first one of the N memory blocks as a current first possible

refresh block (col. 7 lines 17-42), a multiplexer (732, figure 7) for receiving the current first possible refresh block and the current second possible refresh block from the respective address generators, i.e., the multiplexer (732, figure 7) to select either the external access or the internal refreshing operation as an output based on the result of the comparator, (col. 7 line 17 through col. 8 line 14 and col. 9 lines 21-34 and col. 12 line 34-37), external access compare logic (734, figure 7) operable to compare the block of an externally generated access to the current possible refresh block of the first address generator, wherein the apparatus is operable to permit the externally generated access to access the one of the N memory blocks during a certain interval, (col. 7 lines 17 through col. 8 line 19 and col. 9 line 7 through col. 10 line 15), and, the multiplexer is operable to select the at least portion of the current first possible refresh block for refreshing during the certain interval responsive to the external access compare logic indicating that the memory block of the externally generated access does not contend with the current first possible refresh block (col. 9 line 7 through col. 8 line 15), access control logic (728, figure 7) operable for initiating an idle interval responsive to 1) the external access compare logic indicating that the memory of the externally generated access contends with the current first possible refresh block and 2) refresh block compare logic indicating that the current first and second possible refresh blocks are a same one possible refresh block (col. 7 line 17 through col. 8 line 20 and col. 9 line 7 through col. 10 line 15). Although Zheng does not clearly disclosure the second address generator is operable to generate an address of a second one of the N memory blocks as a current second possible refresh block, and a refresh block compare logic operable for checking whether the first and second address generators are currently designating the same possible refresh block, wherein the apparatus is operable to permit the externally generated

access to access the one of the N memory blocks during the certain interval, and the multiplexer is operable to select the at least portion of the current second possible refresh block for refreshing during the certain interval responsive to 1) the external access compare logic indicating that the memory block of the externally generated access contends with the current first possible refresh lock and 2) refresh block compare logic indicating that the current first and second possible refresh blocks are different ones of the N memory blocks, Zheng teaches each of the row control circuit (720, figure 7) in the refresh control circuit (700, figure 7) are able to receive an refresh control signal to provide a refresh address generator and perform a refresh operation in corresponding memory bank (col. 8 line 40 through col. 9 line 34), in addition, Zheng teaches the refresh control circuit can support concurrent memory access and refresh of remaining no-active memory sections, and multiple memory banks can be refreshed at any particular moment concurrently (col. 9 line 66 through col. 10 line 15), thus, Zheng teaches using a row control circuit for each memory bank allows for maintenance of a separate refresh address for each memory bank (col. 8 line 58 through col. 9 line 6), furthermore, Zheng teaches the comparator (734, figure 7) is able to compare the external command and the selected refreshing internal banks, wherein if the external command is the same as the selected refreshing banks, the memory is issued a busy signal in response to the external request which memory access is not permitted, the external circuits then wait until the refresh operation is completed before issuing the memory access command (col. 11 lines 23-56), and the multiplexer to select either the external access or the internal refreshing operation as an output based on the result of the comparator, (col. 7 line 17 through col. 8 line 14 and col. 9 lines 21-34 and col. 12 line 34-37). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to

recognize the computer system of Zheng is able to generate an address of a second one of the N memory blocks as a current second possible refresh block, and the comparator is able to perform the same function of the refresh block compare logic.

Allowable Subject Matter

5. Claims 5-10 and 15-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Rahman et al. (US PAT. 5,873,114) disclosures integrated processor and memory control unit including refresh queue logic for refreshing DRAM during idle cycles (abstact).

Nuwayser (US PAT. 5,265,231) disclosures refresh control arrangement and a method for refreshing a plurality of random access memory banks in a memory system (col. 2 lines 22-52).

Williams et al. (US PAT. 6,400,631) disclosures circuit, system and method for executing a refresh in an active memory bank (abstract).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H Li whose telephone number is 703-305-3846. The examiner can normally be reached on Tue-Fri 9:00 a.m. to 6:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 703-305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Zhuo H. Li

August 20, 2004

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